CLAIMS

1. A process for fabricating a semiconductor substrate with a single-crystal lattice, the process comprising the steps of:

forming a substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface;

amorphizing the single-crystal lattice around a periphery of the recess;

depositing a layer of amorphous material having the same chemical composition as that of the substrate; and

thermally annealing the amorphous material so as to be continuous with the single-crystal lattice of the substrate.

2. The process according to claim 1, further comprising the step of:

planarizing the top surface of the substrate.

3. The process according to claim 2, wherein the step of planarizing the top surface includes planarizing the top surface by a chemical-mechanical polishing.

4. The process according to claim 1, wherein the step of forming the substrate includes forming the substrate with at least part of the material selected from the group of material consisting of silicon, germanium, silicon carbide, and gallium arsenide.

5. The process according to claim 3, wherein the step of amorphizing includes amorphizing with a localized ion implantation around the recess by a masking operation.

6. The process according to claim 2, wherein the step of forming a substrate include the sub-steps of:

depositing a first layer of a first material and a second layer of a second material in succession on the substrate;

etching a trench;

filling trench with a fill material so as to form the single-crystal lattice discontinuity;

etching the first layer and an upper portion of the trench fill material so as to form lateral cavities in the second layer in communication with the trench and so as to form the recess at the discontinuity; and

removing the second layer.

7. The process according to claim 6, wherein the sub-step of filling of the trench with fill material includes filling the trench with at least part of the fill material selected from the group of fill material consisting of silicon, a silicon oxide and a silicon nitride.

8. The process according to claim 6, wherein the sub-step of filling of the trench with fill material includes filling at least part of the trench with an insulating fill material.

9. The process according to claim 6, wherein the sub-step of filling of the trench is carried out by depositing silicon oxide as a conformal coating.

10. The process according to claim 6, wherein the sub-step of filling of the trench is carried out by thermal oxidation of the silicon.

11. The process according to claim 6, wherein the sub-step of etching includes forming a buried capacitor in the trench.

12. The process according to claim 11, wherein the sub-step of etching the trench includes etching a trench with walls and wherein the sub-step of filling the trench further comprises:

lining the walls of the trench with oxide by thermal oxidation;

depositing a highly doped polycrystalline silicon in the trench so as to fill it; and

etching the polycrystalline silicon so that a fill level of the trench is below the surface of the substrate.

13. The process according to claim 6, wherein the sub-step of etching includes forming a buried diode in the trench.

14. The process according to claim 13, wherein the sub-step of filling the trench further comprises:

depositing a highly doped polycrystalline silicon in the trench so as to fill it; and

etching the polycrystalline silicon so that a fill level of the trench is below the surface of the substrate.

15. The process according to claim 6, wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

16. The process according to claim 14, wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

17. An integrated circuit comprising:

a silicon substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface and whereby the surface is treated in accordance with the process of claim 1.

18. An integrated circuit comprising:

a silicon substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface, wherein the single-crystal lattice is amorphized around a periphery of the recess; and

a layer of amorphous material having the same chemical composition as that of the substrate is deposited on the single-crystal lattice which has been amorphized, whereby the amorphous material is thermally annealed so as to be continuous with the single-crystal lattice of the substrate.

19. The integrated circuit according to claim 18, further comprising at least two adjacent transistors formed within the substrate comprising at least one buried trench and the surface of which is made uniform in accordance with the process according to claim 6, the trench forming an isolating trench separating the contiguous buried layers of the transistors.